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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/590,251	08/17/2006	Eddie Huang	GB04 0044 US1	7154
65913	7590	10/16/2009		
NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER NGUYEN, JOSEPH H	
			ART UNIT 2815	PAPER NUMBER
			NOTIFICATION DATE 10/16/2009	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/590,251

Applicant(s)

HUANG ET AL.

Examiner

JOSEPH NGUYEN

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 August 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2 and 4-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-2, 4-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 May 2009 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
- Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 4 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over figures 1-3 of the acknowledged prior art (APA) in view of Saito et al. (U.S. Publication No. 2004/0195618).

Regarding claims 1 and 7, applicant admitted in figures 1-3 of (APA) it is well known in the art that a vertical trench gate semiconductor device (or a method of manufacturing a vertical trench gate transistor semiconductor device) comprising a semiconductor body 2 having a top major surface 2a and a plurality of trench gates comprising trenches 6 extending into the semiconductor body from the top surface with insulated gate electrode 4 therein, the semiconductor body comprising source and drain regions 8, 12 of a first conductivity type which are separated by a channel accommodating region 10 of a second, opposite conductivity type adjacent the trench gates wherein the trench gates extend in stripes (Fig. 1), the source regions extend transversely between the trench gates in stripes, projection of the source stripes across the trench gate defines intermediate trench portions between the projected source stripes. Also see page 2, lines 6-26 of the specification of the instant application.

Figures 1-3 of (APA) do not show mutually spaced regions of the second conductivity type provided immediately below the intermediate trench portions that are connected to source potential, wherein each of said spaced regions extends from the channel accommodating region on one side of a trench to meet the channel accommodating region on the other side of the trench. However, Saito et al. discloses in figure 19 a vertical trench gate semiconductor device comprising mutually spaced regions 14B of the second conductivity type (p type) are provided immediately below the intermediate trench portions that are connected to source potential 13 wherein each of said spaced regions extends from the channel accommodating region 12 on one side of a trench to meet the channel accommodating region on the other side of the trench. In view of such teaching, it would have been obvious at the time of the present invention to modify figures 1-3 of (APA) by including mutually spaced regions of the second conductivity type provided immediately below the intermediate trench portions being connected to source potential wherein each of said spaced regions extending from the channel accommodating region on one side of a trench to meet the channel accommodating region on the other side of the trench so as to improve the function and performance of a trench gate semiconductor device (paragraph [0049]).

Regarding claim 2, Saito et al. discloses in figure 19 each spaced region 14B is an extension of the channel accommodating region 12. Note that the channel accommodating region 12 and the spaced region 14B are both formed of p type and

thus it can be considered that the spaced region 14B is an extension of the channel accommodating region 12.

Regarding claim 4, the combination of figures 1-3 of (APA) and Saito et al. would disclose the depth of each trench oscillates along its length between depths above and below the lower boundary of the channel accommodating region such that the second conductivity type region that provides the channel accommodating region 42 extends periodically below the trench 14B to form the spaced regions.

Regarding claim 8, the claim language is merely product by process limitation because claim 8 depends on product claim 1. MPEP § 2113 states that even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend upon its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product made by a different process. *In re Thorpe*, 777, F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claim 9, Saito et al. discloses in figure 19 each of said spaced regions 14B does not extend into the drain regions 15 of the semiconductor body.

3. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over figures 1-3 of (APA) and Saito et al. and further in view of Hsu et al. (U.S. Publication No. 2004/0145011).

Regarding claims 5-6, figures 1-3 of (APA) and Saito et al. together disclose all steps of the method set forth in claims 5-6. except for the first and second mask being used over a top major surface of the semiconductor body. However, Hsu et al. disclose in figures 2A-2H the first and second mask being used over a top major surface of the semiconductor body (see pages 2-3). Note that the method used to form the device shown in figures 1-3 of (APA) would include the step of forming the trenches deeper than the lower boundary of the channel accommodating region and shallower than said lower boundary between source region stripes, and the method used to form the device shown in figure 19 of Saito et al. would include forming mutually spaced regions 14B of a second conductivity type wherein each of said spaced regions extends from the channel accommodating region on one side of a trench to meet the channel accommodating region on the other side of the trench.

In view of such teaching, it would have been obvious at the time of the present invention to further modify figures 1-3 of (APA) and Saito et al. by using the first and second mask over a top major surface of the semiconductor body so as to effectively form an improved vertical trench gate semiconductor device.

Regarding claim 6, the Examiner takes the Official Notice that it only involves routine skill in the art to have the etchant etches the first mask material more slowly than the semiconductor body, since doing so would preserve the first mask on the top surface until the etching step of the semiconductor body is done such that there would be no undesired etched areas on the top surface of the semiconductor body.

Response to Arguments

4. Applicant's arguments with respect to claims 1-2 and 4-9 have been considered but are moot in view of the new ground(s) of rejection.
5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 8:30 am- 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/J. N./

Examiner, Art Unit 2815

/Kenneth A Parker/

Supervisory Patent Examiner, Art Unit 2815